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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/992,387	11/16/2001	Anthony L. Coyle	50000.2162	7595

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EXAMINER	
LEWIS, MONICA	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 08/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/992,387	COYLE ET AL.	
	Examiner	Art Unit	
	Monica Lewis	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 May 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 17-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 17-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *13 November 2002* is: a)☒ approved b)☐ disapproved by the Examiner

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This office action is in response to the response filed May 30, 2003.

Response to Arguments

2. Applicant's arguments with respect to claims 1-10 and 17-24 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-10 and 17-24 are rejected under 35 U.S.C. 103(a) as obvious over Rahim (U.S. Patent No. 6,362,525) in view of Hino et al. (U.S. Patent No. 6,157,084).

In regards to claim 1, Rahim discloses the following:

a) an integrated circuit chip having an outline, active and passive surfaces, active components including a plurality of contact pads on said active surface (For Example: See Figure 10);

b) a plurality of electrical coupling members (50) (For Example: See Figure 10);

c) an electrically insulating thin-film interposer having first and second surfaces, a plurality of electrically conductive lines integral with said first surface, a plurality of electrically conductive paths extending through said interposer, contacting said conductive lines and forming exit ports on said second surface (For Example: See Figure 10); and

d) chip coupling members attached to said conductive lines, covering an area portion of said first interposer surface (For Example: See Column 8 Lines 11-15).

In regards to claim 1, Rahim fails to disclose the following:

a) contact pads spaced apart by less then 100 um.

However, the applicant has not established the critical nature of the dimension of "contact pads spaced apart by less then 100 um." "The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir.1990).

b) encapsulation material protecting said passive chip surface and at least a portion of said first interposer surface not covered by said attached chip.

However, Hino et al. ("Hino") discloses an encapsulant for a ball grid array package (For Example: See Figure 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Rahim to include an encapsulant as disclosed in Hino because it aids in sealing the element (For Example: See Column 4 Lines 24 and 25).

Additionally, since Rahim and Hino are both from the same field of endeavor, the purpose disclosed by Hino would have been recognized in the pertinent art of Rahim.

c) coupling members selected from a group consisting of gold bumps, copper bumps, copper/nickel/palladium bumps, and z-axis conductive epoxy.

However, Hino discloses the use of gold bumps (For Example: See Column 5 Lines 8-15). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Rahim to include the use of gold bumps as

disclosed in Hino because it aids in providing high connection reliability (For Example: See Column 5 Lines 8-26).

Additionally, since Rahim and Hino are both from the same field of endeavor, the purpose disclosed by Hino would have been recognized in the pertinent art of Rahim.

In regards to claims 2 and 18, Rahim discloses the following:

a) solder balls attached to said exit ports on said second interposer surface (See Figure 10).

In regards to claims 3 and 19, Rahim discloses the following:

a) an adhesive (R) non-conductive polymer underfilling any spaces between said chip coupling members attached to said conductive lines under said chip.

However, Hino discloses the use of polyimide (For Example: See Column 4 Lines 57-67 and Column 5 Lines 1-4). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Rahim to include the use of gold bumps as disclosed in Hino because it aids in providing heat resistance (For Example: See Column 4 Lines 57-67 and Column 5 Lines 1-4).

Additionally, since Rahim and Hino are both from the same field of endeavor, the purpose disclosed by Hino would have been recognized in the pertinent art of Rahim.

In regards to claims 4 and 20, Rahim fails to disclose the following:

a) interposer is a polyimide film.

However, Hino discloses the use of polyimide (For Example: See Column 4 Lines 57-67 and Column 5 Lines 1-4). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Rahim to include

the use of gold bumps as disclosed in Hino because it aids in providing heat resistance (For Example: See Column 4 Lines 57-67 and Column 5 Lines 1-4).

Additionally, since Rahim and Hino are both from the same field of endeavor, the purpose disclosed by Hino would have been recognized in the pertinent art of Rahim.

In regards to claims 5 and 20, Rahim discloses the following:

a) interposer has an outline larger than said outline of said chip (For Example: See Figure 10).

In regards to claims 6 and 22, Rahim discloses the following:

a) electrically conductive lines are made of a material selected from a group consisting of copper, copper alloy, or copper plated with tin, tin alloy, silver, or gold (For Example: See Column 8 Lines 5-8).

In regards to claim 7, Rahim discloses the following:

a) coupling member is interdiffused with said conductive lines (For Example: See Figure 10 and Column 8 Lines 10-15).

In regards to claims 8 and 23, Rahim fails to disclose the following:

a) encapsulation material is a molding compound.

However, Hino discloses an encapsulant for a ball grid array package (For Example: See Figure 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Rahim to include an encapsulant as disclosed in Hino because it aids in sealing the element (For Example: See Column 4 Lines 24 and 25).

Additionally, since Rahim and Hino are both from the same field of endeavor, the purpose disclosed by Hino would have been recognized in the pertinent art of Rahim.

In regards to claims 9 and 23, Rahim fails to disclose the following:

a) molding compound has the same outline as said interposer.

However, Hino discloses an encapsulant for a ball grid array package (For Example: See Figure 1 and Figure 7). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Rahim to include an encapsulant as disclosed in Hino because it aids in sealing the element (For Example: See Column 4 Lines 24 and 25).

Additionally, since Rahim and Hino are both from the same field of endeavor, the purpose disclosed by Hino would have been recognized in the pertinent art of Rahim.

In regards to claim 10, Rahim discloses the following:

a) an integrated circuit chip having an outline, active and passive surfaces, and active components including a plurality of contact pads on said active surface (For Example: See Figure 10);

b) a plurality of electrical coupling members attached to said contact pads (For Example: See Figure 10);

c) an electrically insulating thin-film interposer having first and second surfaces, a plurality of electrically conductive lines integral with said first surface, a plurality of electrically conductive paths extending through said interposer, contacting said conductive lines and forming exit ports on said second surface (For Example: See Figure 10); and

d) chip coupling members attached to said conductive lines, covering an area portion of said first interposer surface (For Example: See Column 8 Lines 11-15).

In regards to claim 10, Rahim fails to disclose the following:

a) encapsulation material protecting said passive chip surface and at least a portion of said first interposer surface not covered by said attached chip.

However, Hino discloses an encapsulant for a ball grid array package (For Example: See Figure 1). It would have been obvious to one having ordinary skill in the art at the time the

invention was made to modify the semiconductor of Rahim to include an encapsulant as disclosed in Hino because it aids in sealing the element (For Example: See Column 4 Lines 24 and 25).

Additionally, since Rahim and Hino are both from the same field of endeavor, the purpose disclosed by Hino would have been recognized in the pertinent art of Rahim.

c) coupling members selected from a group consisting of gold bumps, copper bumps, copper/nickel/palladium bumps, and z-axis conductive epoxy.

However, Hino discloses the use of gold bumps (For Example: See Column 5 Lines 8-15). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Rahim to include the use of gold bumps as disclosed in Hino because it aids in providing high connection reliability (For Example: See Column 5 Lines 8-26).

Additionally, since Rahim and Hino are both from the same field of endeavor, the purpose disclosed by Hino would have been recognized in the pertinent art of Rahim.

In regards to claim 17, Rahim discloses the following:

a) an integrated circuit chip having an outline, active and passive surfaces, and active components including a plurality of contact pads on said active surface (For Example: See Figure 10);

b) a plurality of electrical coupling members attached to said contact pads (For Example: See Figure 10);

c) an electrically insulating thin-film interposer having first and second surfaces, a plurality of electrically conductive lines integral with said first surface, a plurality of electrically conductive paths extending through said interposer, contacting said conductive lines and forming exit ports on said second surface (For Example: See Figure 10); and

d) chip coupling members interdiffused with said conductive lines (For Example: See Column 8 Lines 11-15).

In regards to claim 17, Rahim fails to disclose the following:

a) encapsulation material protecting said passive chip surface and at least a portion of said first interposer surface not covered by said attached chip.

However, Hino discloses an encapsulant for a ball grid array package (For Example: See Figure 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Rahim to include an encapsulant as disclosed in Hino because it aids in sealing the element (For Example: See Column 4 Lines 24 and 25).

Additionally, since Rahim and Hino are both from the same field of endeavor, the purpose disclosed by Hino would have been recognized in the pertinent art of Rahim.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 703-305-3743. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 703-308-4905. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722 for regular and after final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ML
August 8, 2003

Michael Trinh
Primary Examiner
Art SPE